

WHAT IS CLAIMED IS:

1. A computer-aided wiring diagram verifying method of verifying diagram data for a wiring mask including oblique wirings which are formed from
5 layout data of a semiconductor integrated circuit design and via cells which are arranged on the oblique wirings, comprising:
 - a layer defining step wherein different layer numbers are defined by a layer defining unit to
10 oblique wiring diagrams and via cell diagrams which are included in the layout data of the semiconductor integrated circuit design;
 - a first diagram blending step wherein diagram data including the oblique wiring diagrams and the
15 via cell diagrams is fetched from said layout data and the diagrams are blended every same layer number by a first diagram blending unit;
 - an oblique wiring verifying step wherein the oblique wiring diagrams blended in said first diagram
20 blending step are verified by an oblique wiring verifying unit;
 - a second diagram blending step wherein said oblique wiring diagram blended in said first diagram blending step and said via cell diagram are blended
25 and an oblique wiring mask diagram is formed by a second diagram blending unit; and
 - a blended diagram verifying step wherein the

oblique wiring mask diagram blended in said second diagram blending step is verified by a blended diagram verifying unit.

5 2. A method according to claim 1, wherein
 in said first diagram blending step, the
oblique wiring diagrams are fetched and blended and
the via cell diagrams constructed by the via diagrams
and via mat diagrams surrounding them are fetched and
10 blended, and

 in said second diagram blending step, the
oblique wiring diagram blended in said first diagram
blending step and the via mat diagram of said via
cell diagram are blended in an overlapped portion.

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3. A method according to claim 1, wherein in said
oblique wiring verifying step, whether an interval
between the adjacent oblique wiring diagrams violates
an allowable minimum interval value based on a
20 predetermined design rule or not is verified.

4. A method according to claim 1, wherein in said
blended diagram verifying step, whether an interval
between the oblique wiring diagram and the via cell
25 diagram blended on the oblique wiring adjacent to
said oblique wiring diagram violates a predetermined
design rule or not is verified.

5. A method according to claim 4, wherein said oblique wiring diagrams are inclined from horizontal and vertical directions by 45° , said via cell diagram
5 has a rectangular shape exceeding a line width of said oblique wiring, a via cell on the oblique wiring blended in said second diagram blending step has a blended shape such that a corner portion which perpendicularly crosses the oblique wiring direction
10 is projected over the line width of the oblique wiring, and in said blended diagram verifying step, whether an interval between the projecting portion of the oblique wiring due to the blending of the via cells and the oblique wiring diagram adjacent to said
15 projecting portion violates an allowable minimum interval value based on the predetermined design rule or not is verified.

6. A method according to claim 5, wherein in said
20 blended diagram verifying step, if the via cell exists solely adjacent to the oblique wiring, whether an interval between the oblique wiring and a corner edge of said via cell diagram which faces the oblique wiring diagram so as to perpendicularly crosses it
25 violates the allowable minimum interval value based on the predetermined design rule or not is verified.

7. A method according to claim 2, wherein in said
via mat diagram, a wiring overlap which assures a
necessary and sufficient contact area of said via
cell diagram and said oblique wiring is formed around
5 the via.

8. A program for allowing a computer to execute:
a layer defining step wherein different layer
numbers are defined to diagram data of oblique
10 wirings and data of via cell diagrams which are
included in layout data of a semiconductor integrated
circuit design;

a first diagram blending step wherein diagram
data including the oblique wiring diagrams and the
15 via cell diagrams is fetched from said layout data
and the diagrams are blended every same layer number;

an oblique wiring verifying step wherein the
oblique wiring diagrams blended in said first diagram
blending step are verified;

20 a second diagram blending step wherein the
oblique wiring diagram blended in said first diagram
blending step and said via cell diagram are blended,
thereby forming an oblique wiring mask diagram; and

a blended diagram verifying step wherein the
25 oblique wiring mask diagram blended in said second
diagram blending step is verified.

9. A program according to claim 8, wherein
in said first diagram blending step, the
oblique wiring diagrams are fetched and blended and
the via cell diagrams constructed by the via diagrams
5 and via mat diagrams surrounding them are fetched and
blended, and
in said second diagram blending step, said
oblique wiring diagram blended in said first diagram
blending step and the via mat diagram of said via
10 cell diagram are blended in an overlapped portion.
10. A program according to claim 8, wherein in said
oblique wiring verifying step, whether an interval
between the adjacent oblique wiring diagrams violates
15 an allowable minimum interval value based on a
predetermined design rule or not is verified.
11. A program according to claim 8, wherein in said
blended diagram verifying step, whether an interval
20 between the oblique wiring diagram and the via cell
diagram blended on the oblique wiring adjacent to
said oblique wiring diagram violates a predetermined
design rule or not is verified.
- 25 12. A program according to claim 11, wherein said
oblique wiring diagrams are inclined from horizontal
and vertical directions by 45°, said via cell diagram

has a rectangular shape exceeding a line width of
said oblique wiring, a via cell on the oblique wiring
blended in said second diagram blending step has a
blended shape such that a corner portion which
5 perpendicularly crosses the oblique wiring direction
is projected over the line width of the oblique
wiring, and in said blended diagram verifying step,
whether an interval between the projecting portion of
the oblique wiring due to the blending of the via
10 cells and the oblique wiring diagram adjacent to said
projecting portion violates an allowable minimum
interval value based on the predetermined design rule
or not is verified.

15 13. A program according to claim 12, wherein in
said blended diagram verifying step, if the via cell
exists solely adjacent to the oblique wiring, whether
an interval between the oblique wiring and a corner
edge of said via cell diagram which faces the oblique
20 wiring diagram so as to perpendicularly crosses it
violates the allowable minimum interval value based
on the predetermined design rule or not is verified.

25 14. A program according to claim 9, wherein in said
via mat diagram, a wiring overlap which assures a
necessary and sufficient contact area of said via
cell diagram and said oblique wiring is formed around

the via.

15. A computer-aided wiring diagram verifying apparatus for forming diagram data for a wiring mask including oblique wirings and via cells which are arranged on the oblique wirings from layout data of a semiconductor integrated circuit design, comprising:
- a layer defining unit which defines different layer numbers to oblique wiring diagrams and via cell diagrams which are included in the layout data of the semiconductor integrated circuit design;
 - a first diagram blending unit which fetches diagram data including the oblique wiring diagrams and the via cell diagrams from said layout data and blends the diagrams every same layer number;
 - an oblique wiring verifying unit which verifies the oblique wiring diagrams blended by said first diagram blending unit;
 - a second diagram blending unit which blends the oblique wiring diagram blended by said first diagram blending unit and said via cell diagram, thereby forming an oblique wiring mask diagram; and
 - a blended diagram verifying unit which verifies the oblique wiring mask diagram blended by said second diagram blending unit.

16. An apparatus according to claim 15, wherein

said first diagram blending unit fetches and blends the oblique wiring diagrams and fetches and blends the via cell diagrams constructed by the via diagrams and via mat diagrams surrounding them, and

5 said second diagram blending unit blends said oblique wiring diagram blended by said first diagram blending unit and the via mat diagram of said via cell diagram in an overlapped portion.

10 17. An apparatus according to claim 15, wherein said oblique wiring verifying units verifies whether an interval between the adjacent oblique wiring diagrams violates an allowable minimum interval value based on a predetermined design rule or not.

15 18. An apparatus according to claim 15, wherein said blended diagram verifying unit verifies whether an interval between the oblique wiring diagram and the via cell diagram blended on the oblique wiring
20 adjacent to said oblique wiring diagram violates a predetermined design rule or not.

19. An apparatus according to claim 18, wherein said oblique wiring diagrams are inclined from
25 horizontal and vertical directions by 45°, said via cell diagram has a rectangular shape exceeding a line width of said oblique wiring, a via cell on the

oblique wiring blended by said second diagram
blending unit has a blended shape such that a corner
portion which perpendicularly crosses the oblique
wiring direction is projected over the line width of
5 the oblique wiring, and said blended diagram
verifying unit verifies whether an interval between
the projecting portion of the oblique wiring due to
the blending of the via cells and the oblique wiring
diagram adjacent to said projecting portion violates
10 an allowable minimum interval value based on the
predetermined design rule or not.

20. An apparatus according to claim 19, wherein if
the via cell exists solely adjacent to the oblique
15 wiring, said blended diagram verifying unit verifies
whether an interval between the oblique wiring and a
corner edge of said via cell diagram which faces the
oblique wiring diagram so as to perpendicularly
crosses it violates the allowable minimum interval
20 value based on the predetermined design rule or not.

21. An apparatus according to claim 16, wherein in
said via mat diagram, a wiring overlap which assures
a necessary and sufficient contact area of said via
25 cell diagram and said oblique wiring is formed around
the via.